

What is claimed is:

- 1 1. A method, comprising:
2 providing at least one buffer in a memory interface between
3 a chipset and a plurality of memory modules, each module having a
4 plurality of memory ranks, said at least one buffer allowing the
5 memory interface to be split into first and second sub-
6 interfaces, where the first sub-interface is between the chipset
7 and said at least one buffer, and the second sub-interface is
8 between said at least one buffer and the memory modules, such
9 that said at least one buffer provides electrical isolation
10 between the chipset and the memory modules;
11 configuring said at least one buffer to latch data being
12 transferred between the chipset and the memory modules, such that
13 the first and second sub-interfaces operate independently but in
14 synchronization with each other; and
15 interleaving outputs of said at least one buffer.
- 1 2. The method of claim 1, wherein interleaving allows bit
2 numbers required on said second sub-interface to double.

1 3. The method of claim 1, wherein providing at least one
2 buffer isolates the first and second sub-interfaces in such a
3 manner that the first sub-interface is operated at different
4 voltage level than the second sub-interface.

1 4. The method of claim 3, wherein an operating voltage
2 level of said first sub-interface is less than 1.0 volt.

1 5. The method of claim 3, wherein an operating voltage
2 level of said second sub-interface is between 1.2 and 1.8 volts.

1 6. The method of claim 1, wherein providing at least one
2 buffer isolates the first and second sub-interfaces in such a
3 manner that the first sub-interface is operated at a higher
4 frequency than the second sub-interface.

1 7. The method of claim 6, wherein said first sub-interface
2 is operated at twice the frequency of the second sub-interface.

1 8. The method of claim 7, wherein a number of data lines
2 in said first sub-interface is half that of a number of data
3 lines in said second sub-interface.

1 9. The method of claim 1, wherein interleaving outputs of
2 said at least one buffer is provided by connecting the outputs
3 together in a wired-OR mode, and sequentially reading data from
4 the buffer onto a data bus connected to the chipset.

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1 10. The method of claim 1, wherein interleaving outputs of
2 said at least one buffer is provided by multiplexing the outputs,
3 and sequentially outputting data onto a data bus.

1 11. The method of claim 1, further comprising:
2 providing a control logic to coordinate the transfer of data
3 from said at least one buffer in an interleaved mode.

1 12. The method of claim 1, wherein each of said memory
2 modules includes dynamic random access memory (DRAM).

1 13. The method of claim 1, wherein each of said memory
2 modules includes double data rate (DDR) DRAM.

1 14. The method of claim 1, wherein each of said memory
2 modules includes quad data rate (QDR) DRAM.

1 15. A method, comprising:

2 isolating a memory interface between a chipset and at least
3 one memory module, each memory module containing a plurality of
4 memory ranks, where isolating divides the memory interface into
5 first and second sub-interfaces;

6 configuring said first and second sub-interfaces to transfer
7 data between the chipset and said at least one memory module,
8 such that the first and second sub-interfaces operate
9 independently but in synchronization with each other; and

10 interleaving outputs of said plurality of memory ranks,

11 where said first and second sub-interfaces are configured in
12 such a manner that the first sub-interface is operated at a
13 different voltage level and at a higher frequency than the second
14 sub-interface.

1 16. The method of claim 15, wherein said isolating a memory
2 interface is provided by at least one buffer disposed between
3 said chipset and said at least one memory module.

1 17. The method of claim 15, wherein an operating voltage
2 level of said first sub-interface is less than 1.0 volt, and an
3 operating voltage level of said second sub-interface is between
4 1.2 and 1.8 volts.

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1 18. The method of claim 15, wherein said first sub-
2 interface is operated at twice the frequency of the second sub-
3 interface.

1 19. The method of claim 18, wherein a number of data lines
2 in said first sub-interface is half that of a number of data
3 lines in said second sub-interface.

1 20. A system, comprising:
2 a chipset;
3 at least one memory module, each module including a
4 plurality of memory ranks;
5 a memory interface between said chipset and said at least
6 one memory module;
7 at least one buffer disposed in said memory interface to
8 divide said memory interface into first and second sub-
9 interfaces, where said first and second sub-interfaces are
10 configured in such a manner that the first sub-interface is
11 operated at different voltage level and at higher frequency than
12 the second sub-interface, and where multiple outputs of said at
13 least one buffer are interleaved.

1 21. The system of claim 20, further comprising:
2 a control logic to sequentially read said interleaved
3 outputs of said at least one buffer onto said memory interface.

1 22. The system of claim 20, wherein an operating voltage
2 level of said first sub-interface is less than 1.0 volt, and an
3 operating voltage level of said second sub-interface is between
4 1.2 and 1.8 volts.

1 23. The system of claim 20, wherein said first sub-
2 interface is operated at twice the frequency of the second sub-
3 interface.

1 24. The system of claim 23, wherein a number of data lines
2 in said first sub-interface is half that of a number of data
3 lines in said second sub-interface.
